Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (currently amended) A system on a chip (SOC) integrated circuit comprising:

a plurality of logic functions, the plurality of logic functions including a plurality of base functions and a plurality of peripheral functions; and

at least one field programmable gate array (FPGA) cell, coupled to the plurality of peripheral functions, wherein the FPGA cell ~~can be configured~~ is configurable to selectively enable the plurality of peripheral functions in the field to allow access to the plurality of peripheral functions by a customer.

2. (original) The SOC integrated circuit of claim 1 which includes a bus coupled to the at least one FPGA cell.

3. (currently amended) The SOC integrated circuit of claim 2 wherein the FPGA cell ~~can be~~ is programmed to selectively complete connections from the bus to the peripheral functions or selectively tie the peripheral functions to an inactive state.

4. (original) The SOC integrated circuit of claim 3 wherein the FPGA cell programs a register coupled thereto.

5. (currently amended) The SOC integrated circuit on a chip of claim 1 wherein ~~a~~

~~customer can configure~~ the FPGA cell is configurable by a customer.

6. (currently amended) A system on a chip (SOC) integrated circuit comprising:

a plurality of logic functions, the plurality of logic functions including a plurality of base functions and a plurality of peripheral functions;

a plurality of buses; and

a plurality of field programmable gate array (FPGA) cells, each of the plurality of FPGA cells coupled to a portion of the peripheral functions and to one of the plurality of buses, wherein each of the plurality of FPGA cells ~~can be configured~~ is configurable to selectively enable a number of peripheral functions in the field to allow access to the number of peripheral functions by a customer.

7. (original) The SOC integrated circuit of claim 6 wherein the plurality of buses comprises a processor local bus (PLB) and an on-chip peripheral bus (OPB)..

8. (currently amended) The SOC integrated circuit of claim 6 wherein the FPGA cell ~~can be~~ is programmed to selectively complete connections from the bus to the peripheral functions or selectively tie the peripheral functions to an inactive state.

9. (original) The SOC integrated circuit of claim 8 wherein the FPGA cell programs a register coupled thereto.

10. (currently amended) A SOC integrated circuit on a chip (SOC) integrated circuit comprising:

a plurality of logic functions, the plurality of logic functions including a plurality of base functions and a plurality of peripheral functions;

a plurality of buses, wherein the plurality of buses comprises a processor local bus (PLB) and an on-chip peripheral bus (OPB), and

a plurality of field programmable gate array (FPGA) cells, each of the plurality of FPGA cells coupled to a portion of the peripheral functions and to one of the plurality of buses, wherein each of the plurality of FPGA cells ~~can be configured~~ is configurable to selectively enable the portion of peripheral functions in the field to allow access to the portion of peripheral functions by a customer, wherein the FPGA cell ~~can be~~ is programmed to selectively complete connections from one of the plurality of buses to the peripheral functions or selectively tie the peripheral functions to an inactive state, and wherein the FPGA cell is programmed through a register coupled thereto.

11. (original) The SOC integrated circuit of claim 10 wherein the plurality of base functions comprise any combination of:

a processor, a universal interrupt controller, an SDRAM controller, an on-chip controller (OCM), an SRAM, a PLB arbiter, an OPB arbiter, an OPB bridge, and a UART.

12. (original) The SOC integrated circuit of claim 11 wherein the plurality of peripheral functions comprise any combination of:

an external bus controller (EBC), an SDRAM controller, a proprietary function, a peripheral controller, an I^2C interface, and a second UART, a DMA controller, a media access layer (MAL) function, and a plurality of media access controllers (MACs).

13. (new) The SOC integrated circuit of claim 1 wherein the FPGA cell coupled to the plurality of peripheral functions is configured after power-on reset in a customer application.

14. (new) The SOC integrated circuit of claim 13 wherein the SOC integrated circuit is coupled to a companion ROM that stores a programming file that selectively enables the plurality of peripheral functions specific to the customer.

15. (new) The SOC integrated circuit of claim 6 wherein each of the FPGA cells coupled to a portion of the plurality of peripheral functions is configured after power-on reset in a customer application.

16. (new) The SOC integrated circuit of claim 15 wherein the SOC integrated circuit is coupled to a companion ROM that stores a programming file that selectively enables the number of peripheral functions specific to the customer.

17. (new) The SOC integrated circuit of claim 10 wherein each of the FPGA cells coupled to a portion of the peripheral functions is programmed after power-on reset of the system on a chip in a customer application.

18. (new) The SOC integrated circuit of claim 17 wherein the SOC integrated circuit is coupled to a companion ROM that stores a programming file that selectively enables the portion of peripheral functions specific to the customer.

19. (new) The SOC integrated circuit of claim 17 further comprising an enable status register coupled to at least one of the FPGA cells and allowing the determination of which peripheral functions are enabled after power-on reset and before attempting to execute the peripheral functions.